

## REMARKS/ARGUMENT

The Examiner objected to a "listing of references in the specification." The specification mentions and describes one reference (JP 63-283277) at pages 1-2. The same reference was enclosed in an Information Disclosure Statement filed March 29, 2000. A photocopy of that Information Disclosure Statement and reference are enclosed herewith. No fee is due. Also enclosed is a copy of our receipt postcard. Although the Patent Office received the IDS, it has not been acknowledged. The Examiner is requested to sign and initial the enclosed Form PTO-1449 in the usual way and return it to the undersigned.

The specification has been checked and is considered to be in good form for examination and issue.

Claims 1-6 and 10 have been rejected under 35 U.S.C. §102(b) as being anticipated by Nakamura et al. Claim 7 was rejected over Nakamura in view of Sato et al. Claim 8 was rejected over Nakamura in view of Takayama. Claim 9 was rejected over Nakamura in view of Wood et al.

Claims 1-3 have been canceled. Claims 4-8 have been placed in independent form by combining them with the features of their parent claim 2. Other amendments have been made as well. As thus amended, allowance of claims 4-12 is requested, at least for the following reasons.

Regarding claim 4, this claim recites "a delay amount adjusting circuit for canceling the effect of a signal delay taking place in a signal cable connecting the solid state image pickup device to the signal processing circuit." The Examiner argued that the 1H delay circuit (91) shown in Fig. 8 in Nakamura suggested the invention of this claim. The Applicants disagree. The 1H delay circuit in Nakamura is a delay for associating pixels in respective rows for correlation purposes. The 1H delay circuit is neither intended to nor capable of canceling the effect of a signal delay taking place in a signal cable connecting the CCD device to the signal processing circuit. Therefore, allowance of claim 4 is requested.

Regarding claim 5, the Examiner pointed out that Nakamura et al. discloses a white balance adjusting circuit. Claim 5 is being amended in accordance with the description of the second embodiment of the invention at pages 19-25. Thus, claim 5 is being amended to recite that the endoscopic function adjusting circuit comprises at least "a white balance adjusting circuit

for detecting ID information indicative of the wavelength distribution of light emitted by a lamp built into the light source, and automatically setting a white balance state in view of said ID information.”

Regarding claim 6, the Examiner pointed out that the Nakamura reference appears to provide some accommodation for a variation in the number of pixels in a CCD. In response, claim 6 is being amended in accordance with the disclosure of the fourth embodiment at pages 32-37. Thus, claim 6 now recites that the adjusting circuit produces a standard video signal from a reduced number of pixels “by storing dummy pixels in a frame memory to compensate for a reduced number of pixels, and by applying a zoom function to produce said standard video signal from said reduced number of pixels.”

Claims 7, 9 and 10 are submitted to be allowable for their dependency from other allowable claims, as well as patentable subject matter therein.

Regarding claim 8, this claim has been amended in accordance with the description of the third embodiment at pages 26-32. Thus, claim 8 now recites that the motorized bending operation of the endoscopic function adjusting circuit is “interlocked with pan and tilt display functions which compensate for said motorized bending operation.”

New dependent claim 11 recites a feature that was recited in original claim 1. New dependent claim 12 recites a feature disclosed at page 15, lines 2-5.

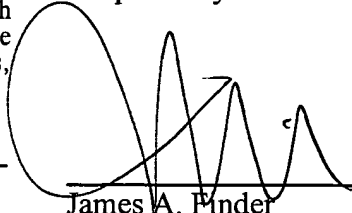
There being no disclosure or suggestion of the foregoing features in the prior art of record, allowance of claims 4-12 is respectfully requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on November 25, 2002:

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Signature  
  
November 25, 2002  
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Date of Signature

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Respectfully submitted,

  
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